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Prospects of Tunnel FETs in the Design of Power Management Circuits for Weak Energy Harvesting DC Sources

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ABSTRACT In this paper, a new tunnel FET (TFET)-based power management circuit (PMC) is proposed for weak dc energy harvesting sources. Thanks to their particular carrier injection mechanisms, TFETs can be used to design efficient energy harvesting circuits by enabling the power extraction from sources which are not only at very low voltage levels (sub-0.1 V) but also at very low power levels (a few nW). As TFET devices are designed as reverse-biased diodes, changes in conventional circuit topologies are required in order to take full advantage of these emerging devices. The circuit design techniques proposed in this paper represent an improvement in output voltage and input power range with respect to previously published TFET-based PMCs. Simulation results show that the TFET-based PMC can sustain itself from a 2.5 nW@50 mV dc source, powering a load at 0.5 V with 29% of efficiency.

INDEX TERMS Boost converter, energy harvesting, low-voltage, nanopower, power management, tunnel FET.

I. INTRODUCTION

Thanks to the miniaturization of embedded systems and the consequent reduction in their power consumption, the harvesting of surrounding energy to directly power the electronics or complement the battery has been a topic of intense research as shown by recent works [1]–[4].

Previous works on power management circuits (PMC) [5]–[8] address low-voltage operation (sub-0.2 V) compatible with weak energy harvesting sources, but their power efficiency when sources with large impedance are considered is very low due to two factors: the minimum power limit required by the controller circuit and losses from power switches at such low voltages.

The Band-to-band Tunneling (BTBT) carrier injection mechanism characteristic of the Tunnel-FET (TFET) device makes it an interesting technology for ultra-low voltage and power conversion. This property enables an inverse subthreshold slope (SS) below 60 mV/dec (at room temperature) and consequently a low leakage current, which improves the device electrical characteristics at sub-0.25 V compared to conventional CMOS devices [9]–[12].

Some works have already shown advantages of using this technology for energy harvesting (EH) applications. TFET-based charge pumps [13] and rectifiers [14] are some examples in which the application of TFETs enable the extraction of power levels in the sub-μW range, where conventional CMOS technologies are shown inefficient.

In [15], a first version of a TFET-based PMC was presented for RF EH sources, showing a good efficiency with RF power levels below -25 dBm. The inductor-based boost converter was able to deliver an average power of 1.1 μW to a load with 500 mV (from an input of 142 mV), with power conversion efficiencies (PCEs) as high as 86%. However, that PMC presented large reverse losses produced by the output transistor in the inductor-based boost converter that limited the $VOUT - Vin$ difference. During the idle state of the PMC, the output transistor (TFET) in the boost converter is reverse biased (the intrinsic p-i-n diode

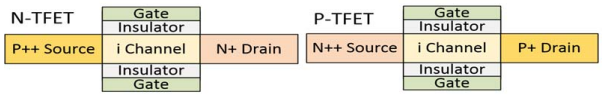

FIGURE 1. Double-gate TFET doping structure.

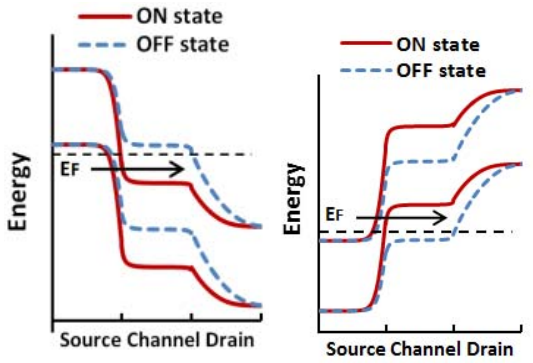

FIGURE 2. (a) *n*-TFET and (b) *p*-TFET energy band diagram under forward bias.

is active) and therefore large voltage differences between the drain and source junctions of that TFET (output *VOUT* and switching node *Vin* of the converter) resulted in a PMC with large reverse losses constraining its voltage and power operation. In order to counteract this effect and allow a TFET-based PMC with a wider voltage/power operation than that previously presented in [15], changes in the inductor-based boost converter and respective controller are required. This work presents circuit design techniques that improve the conversion efficiency of TFET-based PMC interfacing weak energy harvesting sources.

In order to explore the performance of TFETs in the conversion process of ultra-low voltage (sub 0.1 V) and power (nW) sources, both the controller and boost converter presented in [15] are here redesigned and improved in terms of power conversion efficiency. In contrast to the previous work, this one focuses on dc sources with large impedance values, thus requiring a different PMC for impedance matching.

The structure of this work is as follows: in Section II the main electrical characteristics of TFET devices are summarized; Section III describes the behavior of the proposed TFET-PMC; Section IV presents the simulation results; and finally Section V presents the main conclusions of the work.

II. TUNNEL FET CHARACTERISTICS

In contrast with conventional CMOS devices, TFETs are designed with different doping types in the source and drain regions (see Fig. 1). This characteristic results in particular carrier injection mechanisms when the device is forward or reverse biased [9]–[11].

As shown in Fig. 2, under forward bias conditions the current of *n* and *p*-type TFETs are respectively characterized by electron and hole-BTBT. Electron-BTBT occurs when

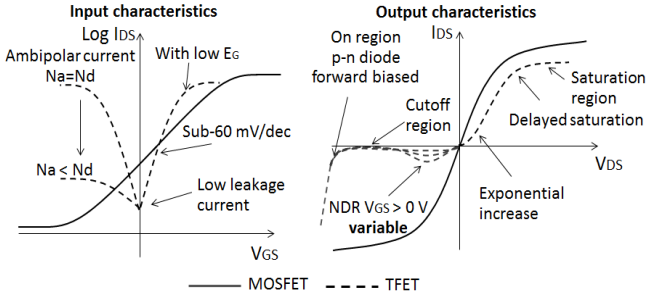

FIGURE 3. Comparison of input (left) and output (right) electrical characteristics between conventional MOSFETs and TFETs.

both drain and channel regions present larger potential levels than that of the source. In contrast, hole-BTBT occurs when both drain and channel potential are lower than that of the source.

A. TFET ELECTRICAL CHARACTERISTICS

The main electrical characteristics of TFETs are presented in Fig. 3 and compared with those of conventional MOSFETS (*n*-type as reference). The dominant BTBT carrier mechanism instead of thermal emission over a potential barrier enables an SS below 60 mV/ dec at room temperature observable in the input characteristic. This property allows the design of efficient circuits at low bias. In addition, the low leakage current of TFETs enable the design of circuits with extremely low idle power consumption.

The particular doping structure of TFETs also produces a different output characteristic when compared to conventional MOSFETs. As shown in Fig. 3 (right), the reverse current of reverse biased TFET follows the characteristic of a diode (the intrinsic p-i-n structure is forward biased). At low reverse bias magnitude ($V_{DS} < 0$ for *n*-TFETs and $V_{DS} > 0$ for *p*-TFETs) the negative differential resistance (NDR) region (and reverse current) can be controlled by changing the gate voltage of the TFET [15]. In contrast, at large reverse bias ($VDS \ll 0$ for *n*-TFETs and $V_{DS} \gg 0$ for *p*-TFETs) the gate magnitude has a negligible effect on the magnitude of reverse current.

This property of TFETs under reverse bias presents a challenge in the design of inductor-based boost converters: when the output TFET-device is reverse biased the conduction of reverse current degrades the conversion efficiency of the circuit, thus limiting the operating voltage range. In order to counteract this effect, the following section presents circuit solutions that alleviate the reverse losses, thus extending the voltage and power operation of inductor-based boost converters designed with TFETs.

B. TFET MODELS USED IN THIS WORK

The use of low energy band gap materials such as InAs or GaSb largely improve the current at low bias. Thus, the choice of III-V based TFETs was proven advantageous in EH applications as opposed to silicon based TFETs, as shown in [13] and [14].

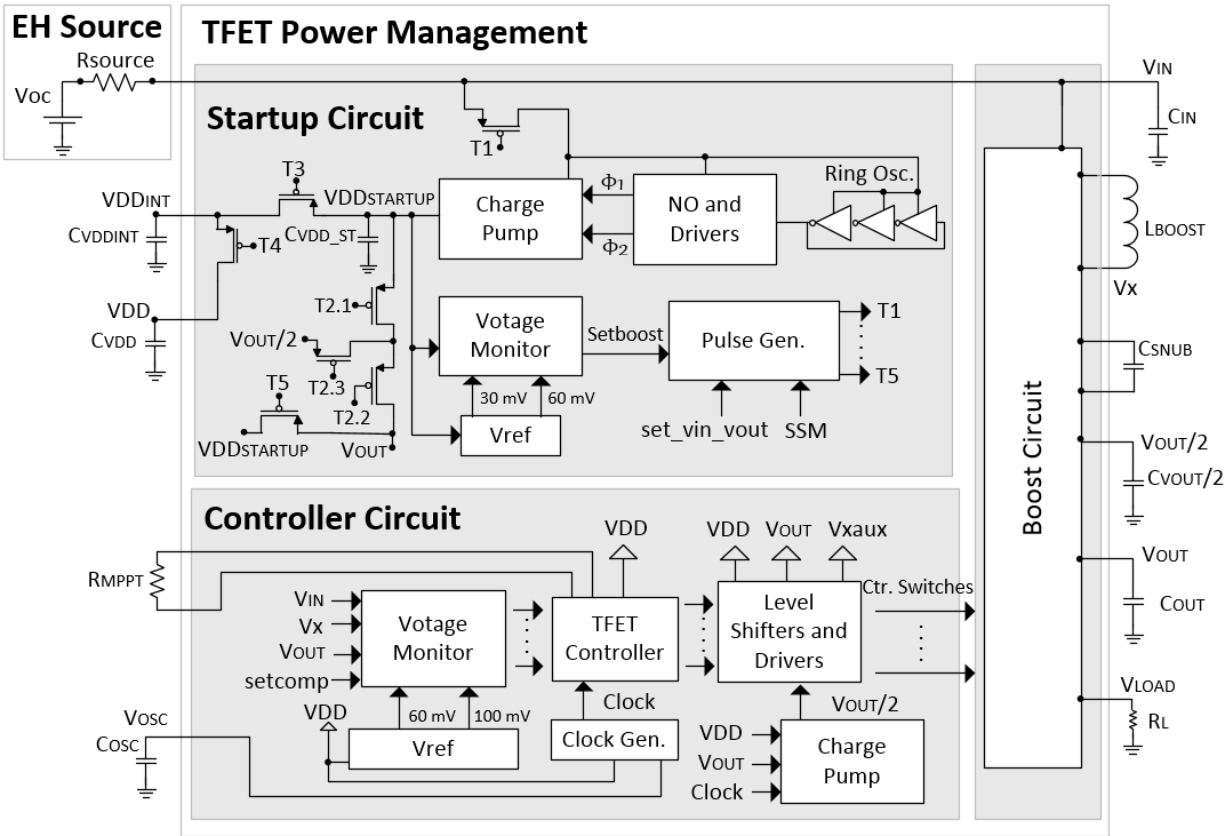

FIGURE 4. **Top level architecture of the proposed TFET-based PMC for ultra-low voltage/power dc sources.**

All the results presented in this work are based on look-up table models describing the electrical characteristics (current and capacitance) of a double-gate GaSb-InAs near broken gap heterojunction TFET with a gate length of 40 nm. The current and capacitance-voltage characteristics were obtained from the TCAD Sentaurus device simulator by the NDCL group from the Pennsylvania State University. More information about this model can be found in [16]. The look-up tables present the current and intrinsic capacitances (CGS and CGD) of the TFET device for each VGS and VDS value (each one from −0.8 V to 0.8 V with 10 mV of interval between points).

III. PMC FOR ULTRA-LOW POWER SOURCES

In this section, a power management circuit (PMC) is proposed and designed to interface with weak EH sources that not only present low input voltage (sub-0.1 V) but also ultra-low power levels (a few nW). In Fig. 4, the top level architecture of the system is shown, comprising three different modules: Startup, Controller and Boost circuit. On a cold start, the Startup circuit slowly charges a capacitor until sufficient voltage is achieved for powering the Controller and thus starting synchronous mode of operation (DCM–Discontinuous Conduction Mode). In DCM operation the Boost module charges a capacitor COUT, and once this capacitor reaches a pre-set value, it is connected to the load, providing the collected energy and disconnecting it once COUT is discharged to some other pre-set voltage. This is repeated cyclically as enough energy is accumulated in COUT. Once the load is enabled for the first time, the PMC starts to operate in self-sustaining mode (SSM), i.e., the storage capacitors in the Startup module that were previously charged by the source *Vin* are then charged by *VOUT*. For maximum power transfer between the power source and the PMC, the boost converter adapts its input impedance to the impedance of the source.

In the following sub-sections, the main modules of the proposed architecture are described. Table 1 shows a description for the main nets and associated storage capacitors in the different modules presented in this paper.

A. STARTUP CIRCUIT MODULE

The Startup module is responsible for powering the Controller module (node *VDD* and storage capacitor CVDD.) The principle of operation of the TFET-based startup module is based on the circuit proposed in [15].

Initially, DCM operation is disabled until $VDD_{startup}$ reaches a pre-required value set as 200 mV. During the cold start phase of the PMC, the voltage at this node increases by using the charge-pump circuitry powered from the EH source. During this phase, the voltage monitor shown in Fig. 5 is required to maintain the voltage of node $VDD_{startup}$

TABLE 1. Glossary of the main nets in the different modules.

Net	Storage Cap.	Module	Description
Vin	CIN	Startup, Boost	Input voltage generated by the energy harvester. Power source for the boost converter and, during startup phase, charge pump.
$VDD_{startup}$	CVDD_st	Startup	Power supply for startup module blocks. Derived from *Vin* during the startup phase, and from V_{OUT} during the self-sustaining mode (SSM) phase.
VDD_{int}	CVDDint	Startup	Connected to $VDD_{startup}$. Auxiliary capacitor used to charge CVDD whenever CVDD_ST is not ready (still being charged).
VDD	CVDD	Startup	Power supply for Controller responsible for DCM operation.
$VOUT$	COUT	Startup, Boost	Output voltage from Boost converter during DCM operation. During startup, connected to $VDD_{startup}$.
Vload	–	Boost	Power supply for the load. Intermittently connected to V_{OUT}.
setboost	–	Startup	Active when $VDD_{startup}$ reaches 200 mV, marks beginning of DCM operation.
set_vin_vout	–	Startup	Active when *setboost* is active, disconnects $VOUT$ from charge pump and connects VDD to start DCM operation.
outcomp	–	Controller	Comparator output between $VOUT$ and $VREF$.
SSM	–	Startup	Active when *outcomp* is active, stops the charge pump and connects $VDD_{startup}$ to $VOUT$, then entering SSM phase.
Vx	–	Boost	Switching node. Controller module monitors this voltage for appropriate DCM operation.
Vosc	–	Controller	Clock waveform. Frequency determined by COSC.
Vx_aux	–	Controller	Driver voltage for switching Vctrp1 in Fig. 8. Connected to either *Vin* or *Vx*.
setcomp	–	Controller	Comparators enable during phase $\Delta T2$.

around 200 mV, either by charging CVDD_ST from the EH source (during cold and DCM phases) or from *VOUT* during SSM phase.

The VDD node is powered by node $VDD_{startup}$ whenever this has enough voltage (at least 200 mV). If $VDD_{startup}$ is being charged, then VDD node is powered by the auxiliary capacitor connected to node VDDint.

A digital signal *SSM* (Self-Sustaining Mode) is triggered when the load is first connected to the PMC (when *VOUT* reaches a pre-required value). After this signal is enabled, the charge-pump circuitry is deactivated and the output capacitor of the PMC (COUT) acts as the power source of the startup module.

Prior to the boost conversion operation, CIN is charged up to the open-circuit voltage (VOC) value of the EH source and COUT is charged to the value of $VDD_{startup}$ (still less than 200 mV) by the TFET switches controlled by T2.1, T2.2 and T2.3. In the RF PMC presented in [15] there is a single p-TFET device between the $VDD_{startup}$ and *VOUT* nodes. When DCM operation starts, *VOUT* is disconnected from $VDD_{startup}$ and its voltage increases beyond the value of $VDD_{startup}$ so that there is a reverse bias of the p-TFET in OFF state. If this difference is large enough, leakage can be important and reverse current degrades the performance of the startup module. For this reason, a possible solution to reduce the reverse losses is to split the p-TFET switch in two different TFETs, with a voltage applied between them (for example half the voltage of node *VOUT*) in order to reduce the reverse bias of each device and the associated reverse losses.

B. TFET-BASED BOOST CIRCUIT

The boost converter must adapt its input impedance to the impedance of the EH source for maximum power transfer and at the same time increase the output voltage to the level

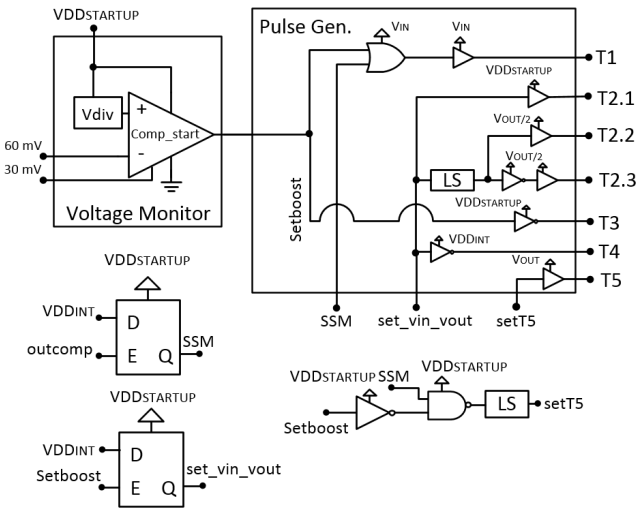

FIGURE 5. Digital and Analog circuitry of the proposed TFET-based startup circuit.

required by the load. In Fig. 6 (Top), it is shown the TFET-based boost converter topology presented in [15]. This circuit presents a good performance with RF EH applications at μW power levels.

Since TFETs are constructed as gated reverse biased p-i-n diodes, one of the main challenges in the design of TFET-based boost converters is to minimize the reverse current conducted by the output transistor S4 during its reverse bias state, i.e., when the inductor is being charged (considered as time interval $\Delta T1$) and when the boost converter is in the idle mode (considered as time interval $\Delta T3$).

In Fig. 7 it is shown that large differences between the output and switching nodes of the boost converter results in a largely reverse biased TFET (device S4) and consequent reverse losses, thus limiting the voltage operation of the

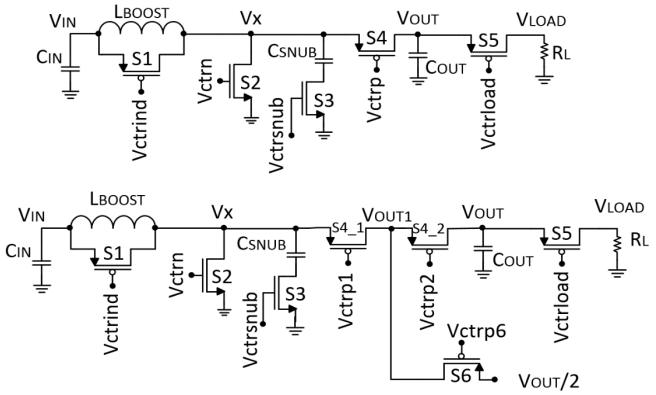

FIGURE 6. Top: Conventional and Bottom: proposed TFET-based boost converter.

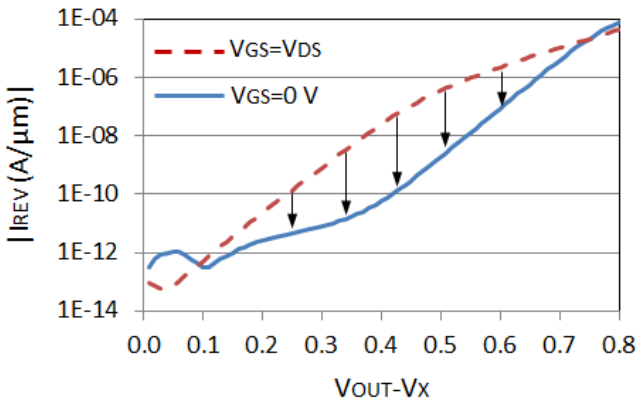

FIGURE 7. Reverse current of S4 in Fig. 6 (Top) considering VGS = 0V and VGS = VDS.

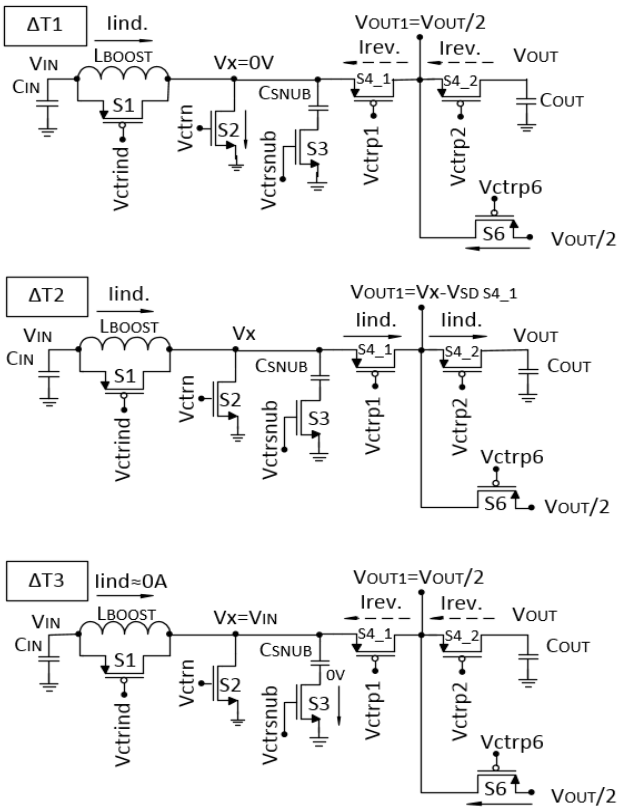

FIGURE 8. Operation states of the proposed TFET-based boost converter.

conversion circuit. In a reverse biased TFET device, applying a gate voltage equal to the source (VGS = 0V) can reduce the reverse current of the device over a wide voltage range when compared to a gate magnitude equal to *VOUT* (VGS = VDS).

In [15], it is shown that increasing the size of the heterojunction TFET S4 results in a trade-off between the decrease of the resultant forward losses and increase of reverse losses. Consequently, there is an optimum size of S4 that minimizes the conversion losses and increases the boost efficiency for different levels of input power. However, if input power varies in time it is not possible to have an optimum sizing. For this reason, changes in the boost converter are proposed and shown in Fig. 6 (Bottom).

As shown in Fig. 8, during the time interval $\Delta T1$ the TFET device S2 is closed and the inductor is charged. The snubber circuit is deactivated, the device S1 is open (off-state) and the voltage at node *Vx* is approximately 0 V. In order to avoid large reverse losses coming from the output devices S4_1 and S4_2, the TFET device S6 is closed and a voltage equal to half the voltage of node *VOUT* is applied to node *VOUT*1. This alleviates the losses of reverse biased transistors S4_1 and S4_2 by reducing their reverse bias magnitude. The VGS applied to both transistors is 0 V in order to reduce the reverse current and consequent reverse losses.

During the time interval $\Delta T2$, the devices S1, S2, S3 and S6 are in off-state and the output transistors S4_1 and S4_2 are closed. The output capacitor is charged by the inductor current up to the voltage value of the switching node *Vx*.

During the idle time $\Delta T3$ of the boost converter, the input (S2) and output transistors (S4_1 and S4_2) operate in off-state, with a voltage applied between the two output transistors to reduce their reverse bias magnitude and conduction of reverse current. In order to attenuate the current in the inductor and avoid large oscillations in the *Vx* node, during $\Delta T3$ the TFET device S1 and the snubber circuit are activated.

The inductor-based boost converter sequence operation is repeated until the voltage at node *VOUT* reaches a pre-required value. Only then the TFET device S5 shown in Fig. 6 (Bottom) is closed and an external load activated. The TFET device S5 remains closed until the voltage at node *VOUT* decreases below a pre-determined threshold point.

In Fig. 9, one can see the sequence of signals applied to the boost converter operating in discontinuous conduction mode. In order to avoid large reverse losses, the boost controller imposes VGS = 0 V to all the TFETs operating during their off-state (reverse biased).

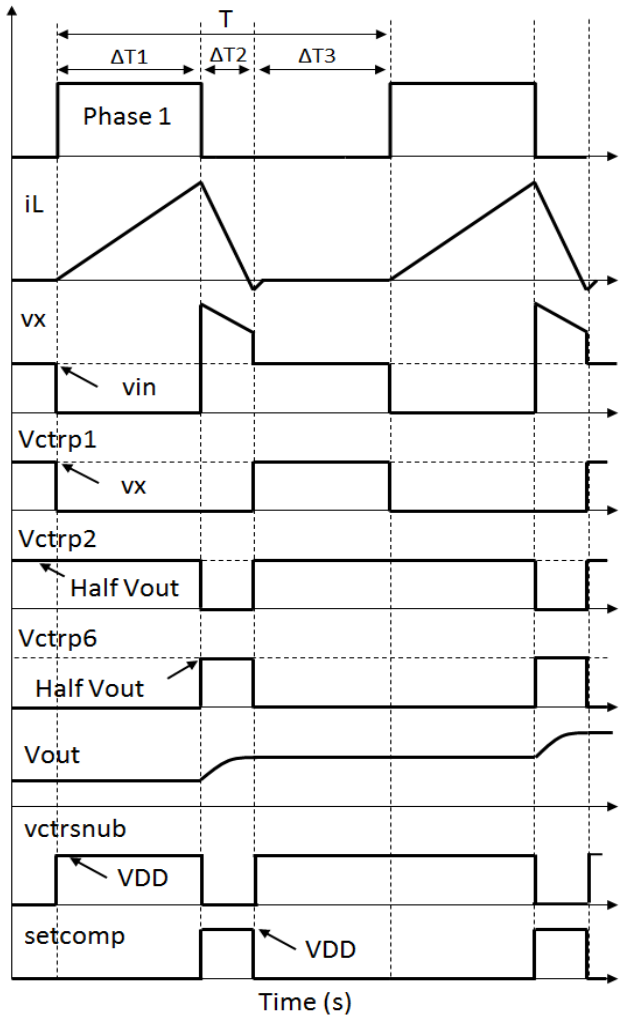

FIGURE 9. Operation sequence of the main electrical signals applied to the proposed boost converter.

C. TFET-BASED CONTROLLER CIRCUIT

In Fig. 10 it is depicted the proposed TFET-based controller responsible for providing the control signals applied to the boost converter shown in Fig. 6 (Bottom). The controller imposes VGS = 0 V to all the reverse biased TFETs presented in the digital and analog cells, and also to the TFET switches in the boost converter. This behavior reduces the reverse losses suffered by reverse biased TFETs, thus increasing the PMC efficiency [15].

An SR (Set-Reset) latch is responsible for controlling the signals applied to the two output transistors presented in the boost converter. A comparator is required to detect the moment when the inductor current is negative, triggering a Reset signal that is applied to the SR latch. Depending on the state of the control signal applied to the input transistor S2 (*Vctrn*) the output transistors S4_1 and S4_2 are conducting or blocking current according to the control signals *Vctrp1* and *Vctrp2*.

A second comparator is required to control the device S5 when the output node *VOUT* reaches a pre-required value,

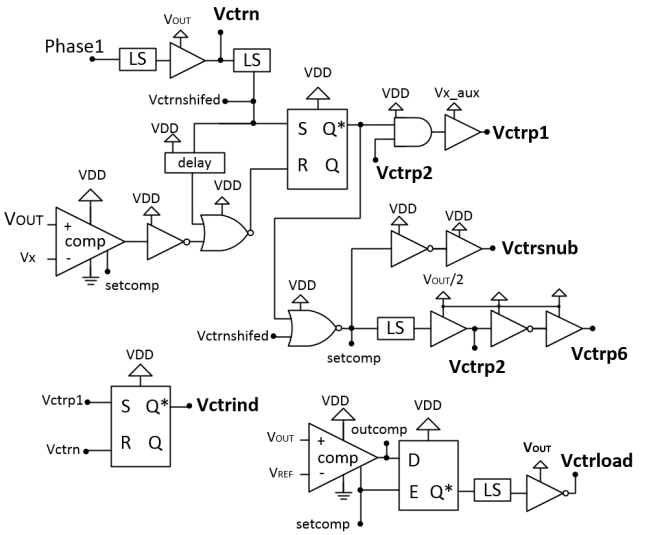

FIGURE 10. Proposed TFET-based controller circuit for the boost converter.

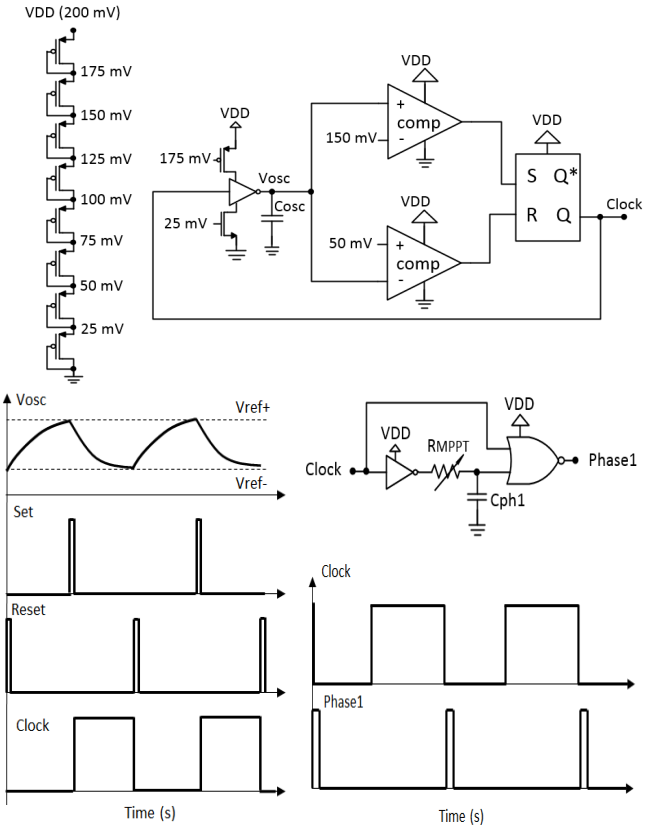

FIGURE 11. Circuits of Clock and Phase 1 signals.

thus enabling a load with the control signal *Vctrload*. In order to maximize the controller efficiency, the two comparators only operate during $\Delta T2$ (*setcomp* active).

As explained in [15], heterojunction TFET-based digital gates are very sensitive to mismatches between digital levels and power supply. Therefore, level shifter (LS) blocks presented in the TFET-based controller are required in order

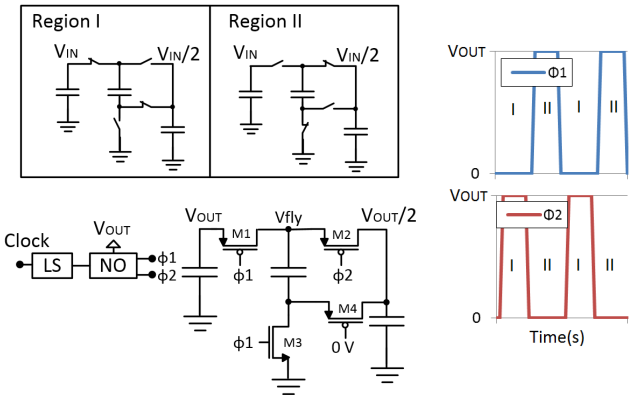

FIGURE 12. Proposed TFET-based voltage divider charge pump.

TABLE 2. Bias conditions of TFETs applied to the voltage divider CP.

Region:	I		II	
M1 (p)	on	$VGS = -VOUT$ $VDS < 0$	off	$VGS \approx 0$ $VDS < 0$
M2 (p)	off	$VGS \approx 0$ $VDS < 0$	on	$VGS = -VOUT/2$ $VDS < 0$
M3 (n)	off	$VGS \approx 0$ $VDS > 0$	on	$VGS = VOUT$ $VDS > 0$
M4 (p)	on	$VGS = -VOUT/2$ $VDS < 0$	off	$VGS \approx 0$ $VDS > 0$

to match the input signals of the digital cells with their power supply voltage. The LS insertion is shown to substantially reduce the power consumption of such cells.

In order to achieve a synchronous boost conversion operation, a clock signal is required. The relaxation oscillator shown in Fig. 11 is responsible for generating a clock signal with a frequency controlled by the capacitor COSC. The RMPPT is responsible for adjusting the duty cycle of the Phase1 signal that triggers the *Vctrn* signal applied to the input transistor S2 of the boost converter. The $VOUT/2$ source is generated by a voltage divider charge pump. The proposed circuit shown in Fig. 12 adapted for TFET operation requires two non-overlapped clock signals generated by a non-overlapped NO circuit powered by *VOUT*. In order to improve the conversion efficiency, the reverse biased TFETs during each region of operation are biased with VGS = 0 V (see Table 2).

IV. SIMULATION RESULTS

This section presents the simulation results of the TFET-based PMC circuit shown in Fig. 4 for ultra-low power dc sources.

In order to extract the maximum power from an EH source, the input impedance of the boost converter should equal the impedance of the source. In an ideal boost converter, the input impedance can be expressed by eq. (1):

$$Z_{IN} = \frac{2L}{t_1^2 f_s}\left(1 + \frac{V_{IN}}{V_{OUT} - V_{IN}}\right)^{-1} \quad (1)$$

In this work, the EH source is simulated with two different impedances, 1 M Ω and 100 k Ω. When considering a fixed

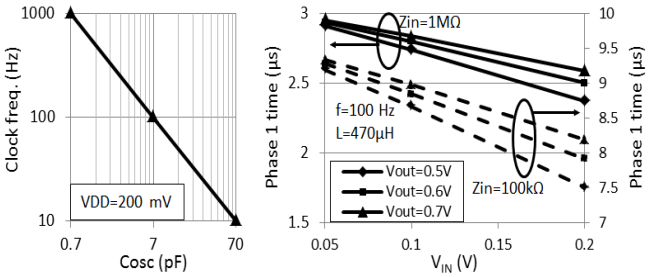

FIGURE 13. Left: Clock frequency of the boost converter in function of Cosc. Right: Phase 1 time required for maximum power transfer considering two different input impedances (ZIN = 1MΩ and ZIN = 100 kΩ). L = 470 μH, f = 100Hz.

inductor L, fixed boost frequency f_s, and $VOUT \gg VIN$, the input impedance of the boost converter can be controlled by t1, i.e., the on-time of the input transistor S2. As expressed by eq. (2), the inductor current and the inductance value are inversely proportional.

$$i_L = \frac{V_{IN} t_1}{L} \quad (2)$$

Therefore, in order to avoid large forward losses in the switches of the boost converter, a large inductor size is desirable. In this work, an inductor with 470 μH and a boost frequency of 100 Hz are considered.

As shown in Fig. 13 (Left), a COSC value of 7 pF in the clock circuit is needed to obtain the desired clock frequency of 100 Hz. In Fig. 13 (Right), the t1 required for different input voltage levels is presented. For a source impedance of 1 MΩ and 100 kΩ, RMPPT values (shown in Fig. 11) of respectively 3.8 MΩ and 14 MΩ are shown to be adequate for maximum power transfer in the considered *Vin* and *VOUT* ranges (50-200 mV and 500-700 mV respectively.) If the impedance of the EH source changes, the RMPPT has to change accordingly. In this work and for simulation simplification, the dc EH source is simulated with fixed impedance.

In Fig. 14, the performance of the conventional and proposed TFET-based boost converters shown in Fig. 6 is compared considering a source with 1 MΩ and different input voltage values. A load of 6.25 MΩ, 25 MΩ and 100 MΩ is enabled (for input power levels of respectively 40 nW, 10 nW and 2.5 nW) when the output voltage of the boost converter reaches a threshold value of 515 mV. One can observe that in the boost converter topology presented in [15] Fig. 6 (Top), there is an output transistor size (S4 width) that minimizes the losses (Forward + Reverse). These losses are presented as a percentage of the total input power Pin. In contrast, the proposed TFET-based boost converter shown in Fig. 6 (Bottom) allows for the reduction of forward losses with larger S4 sizes (WS4_1 + WS4_2), maintaining low reverse losses.

As an example, the performance of the conventional boost converter with an input voltage of 100 mV and output voltage of 500 mV is degraded due to the large reverse

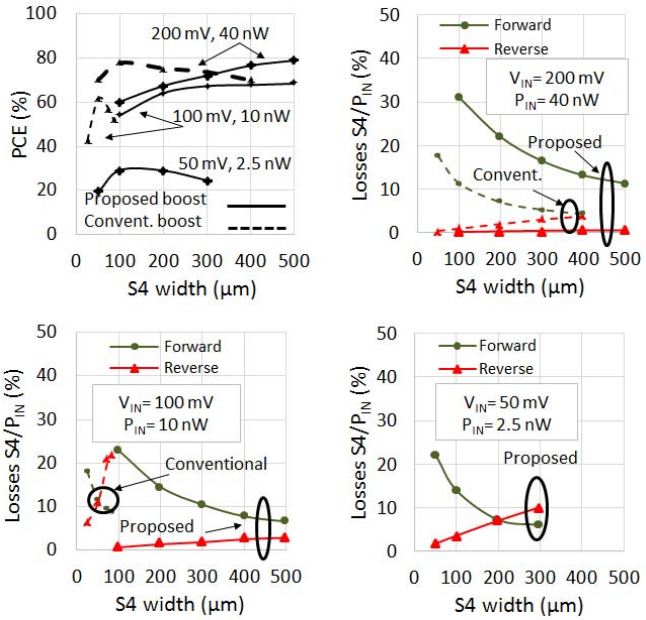

FIGURE 14. **Performance of the conventional and proposed TFET-based boost converters considering an energy harvesting source with 1M Ω. L = 470μH, WS1 = 5μm, WS2 = 1mm, WS3 = 10μm, WS5 = 50μm. WS6 = 200μm, Cin = Cout = 0.1μF, Csnub = 1pF, Vout = 500mV.**

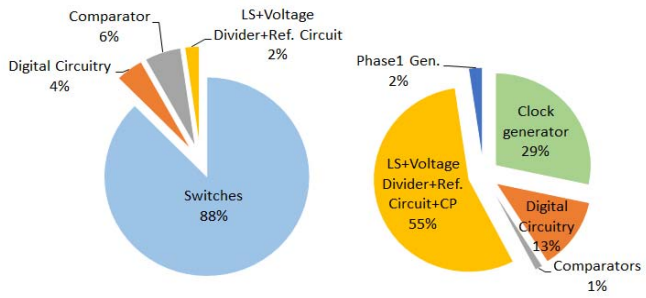

FIGURE 15. **Distribution of power losses in the proposed TFET-based startup and controller circuits.**

losses suffered by the output transistor when reverse biased (VDS = 0.5 V during $\Delta T1$ and VDS = 0.4 V during $\Delta T3$). In contrast, in the presently proposed converter, S4_1 and S4_2 have a reverse bias of VDS = 0.25 V during $\Delta T1$ and S4_1 (S4_2) with VDS = 0.15 V (VDS = 0.25 V) during $\Delta T3$, thus reducing the reverse current and consequent reverse losses.

Note that for an input voltage of 50 mV it is not possible to reach the required 500 mV output voltage for the conventional boost converter due to losses, and consequently this curve is not shown in Fig. 14. The proposed boost converter allows the conversion of such low voltages.

The combination of sub-nW power consumption of the TFET-based startup (614 pW) and controller circuits (580 pW) shown in Fig. 15 and the decrease of reverse losses in output transistors S4_1 and S4_2 allow the proposed boost converter to operate with input power levels as low

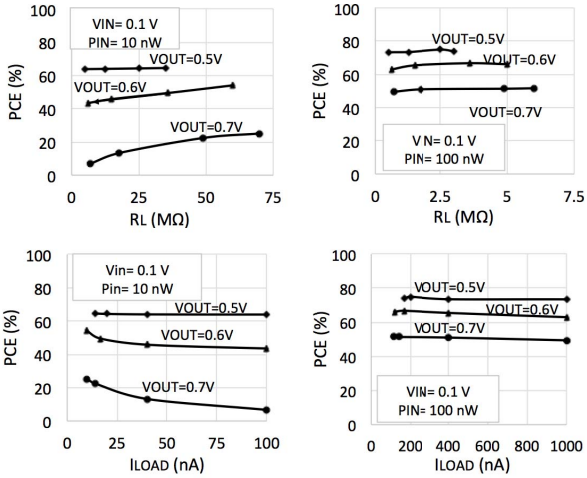

FIGURE 16. **Performance of the proposed TFET-based boost converter for different voltage conversion ratios. WS4 = 200 μm (WS4_1 = WS4_2 = 100 μm).**

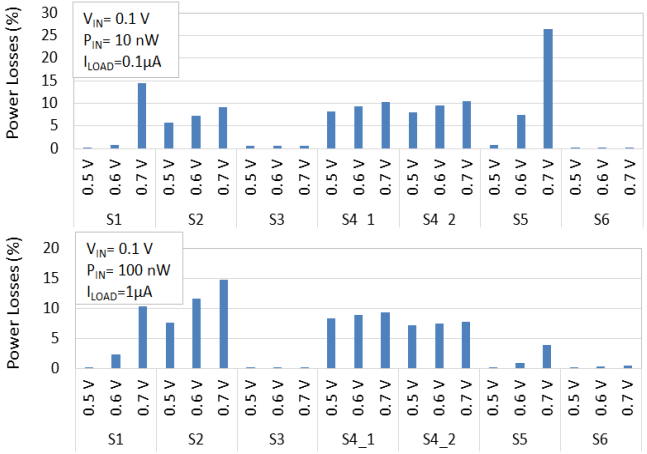

FIGURE 17. **Distribution of losses in the proposed boost-converter for different conversion ratios (*Vin* = 0.1 V, Vout = 0.5V, 0.6V and 0.7V) considering an output load of 100 nA (for Pin = 10 nW) and 1μA (for Pin = 100 nW).**

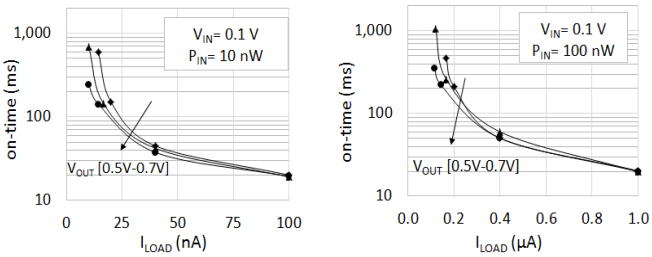

FIGURE 18. **Load on-time for different input power levels and output voltage.**

as 2.5 nW with 29% of power conversion efficiency (PCE) when considering *Vin* = 50 mV and *VOUT* = 0.5 V.

Fig. 16 shows the performance of the proposed TFET-based boost converter, considering an output transistor S4 (S4_1+S4_2) with a width of 200 μm. For an input power

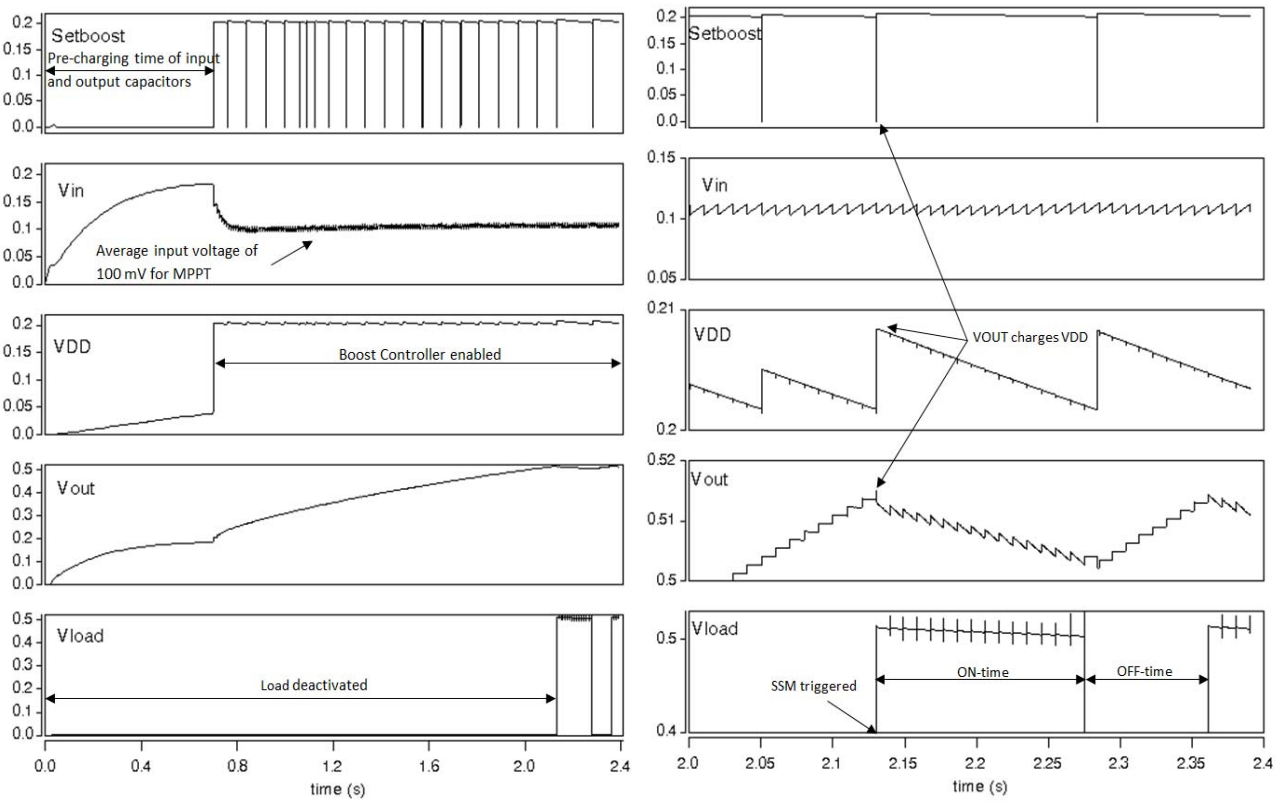

FIGURE 19. **TFET-based PMC transient behavior for Pin = 10 nW, *Vin* = 0.1 V, Vout = 0.5 V, Rload = 25 Mi, L = 470 μH, Cin = Cout = 0.1 μF, WS4_1 = WS4_2 = 200 μm.**

TABLE 3. **Comparison with measured results from recently published power management circuits.**

Ref.	[5]	[6]	[7]	[8]	This work
Tech.	130 nm CMOS	65 nm CMOS	180 nm CMOS	320 nm CMOS	40 nm TFET
Year	2010	2013	2016	2016	2017
Battery for Start-up	Yes (ext. capacitor)	No	No	No	No
$VOUT$	1V	1.2V	3V	1V	0.5-0.7V
PCE	37% @50mV/370nW 68% @100mV/6.8W	70% @50mV/403μW	40% @360mV/10nW 75% @360mV/100nW	50% @124mV/10.5μW	29% @50mV-500mV/2.5nW 50% @100mV-700mV/100nW
Energy Source	Thermal	Thermal	Solar	Solar	dc source

of 10 nW (Vin = 0.1 V, RSOURCE = 1 MΩ) the boost converter is simulated with CIN = COUT = 0.1 μF. For an input power of 100 nW (Vin = 0.1 V, RSOURCE = 100 k Ω) the capacitance values of CIN and COUT are simulated as 1 μF. The results show that the proposed circuit is able to increase a low input voltage value of 0.1 V up to 0.7 V.

The distribution of power losses in the boost converter is presented in Fig. 17 ($IOUT$ = 100 nA for PIN = 10 nW and IOUT = 1 μA for PIN = 100 nW). One can observe that when the input power is low, larger output voltage values lead to larger losses in the TFET switches S1 and S5. When the load is not enabled, the increase of VSD in S5 (with the increase of output voltage) results in an increase of leakage current and consequent power losses. The switch S1 is also shown to be an important source of power losses. During $\Delta T2$, the increase of voltage at node Vx (with larger output voltage values) imposes a high reverse bias in this TFET device, thus increasing its reverse losses.

Fig. 18 presents the load on-time for different input power levels and output voltages. It is shown that an EH source delivering 10 nW (Vin = 0.1 V) to the TFET-based PMC can enable a load with 100 nA ($VOUT$ = 0.7 V) during 20 ms, i.e., two conversion cycles of 10 ms. A similar value is achieved for a load of 1 μA and a source of 100 nW.

In Fig. 19 the transient simulation of the PMC is presented, considering an EH source with an open circuit voltage of 200 mV and 1 MΩ. With maximum power point tracking, the input impedance of the boost converter equals the impedance of the source and an input voltage VIN of 100 mV (PIN = 10 nW) is observed. It is shown that prior to the boost conversion operation the input CIN and output capacitor COUT of the boost converter are pre-charged to a

value close to that of the open circuit voltage of the source and $VDD_{startup}$ respectively. Once charged, the power supply node of the controller is enabled (VDD) and the boost converter starts a synchronous mode of operation. When the output voltage node *VOUT* reaches a threshold value of 515 mV a load is enabled until the capacitor at the output voltage node discharges below a threshold voltage of 500 mV. When the load is enabled for the first time, the circuit enters in a self-sustaining mode (SSM) of operation, i.e., the output capacitor is responsible for charging the capacitors of the startup circuit and controller.

In Table 3, a comparison between the performance of the proposed TFET-based PMC and recent power management units from the literature is presented. The use of III-V heterojunction TFETs in PMCs shows promising results for the energy harvesting field at ultra-low power levels (less than 10 nW.)

V. CONCLUSION

This work presents the design of a TFET-based startup and controller circuits with power consumption as low as 1.2 nW. Such low power enables a boost conversion of 50 mV to 500 mV from weak dc power sources (2.5 nW considered in this work). This example shows the potential for III-V heterojunction TFET technology for efficient power management units for energy harvesting applications in the nW range.

Reverse current in reverse biased TFETs (when the intrinsic p-i-n diode is forward biased) presents a challenge in the design of TFET-based circuits and inductor-based boost converters when compared to the use of conventional thermionic technologies. The reduction of the VGS magnitude in reverse biased TFETs is shown as a good practice to attenuate the reverse losses in TFET-based circuits.

In conventional inductor-based boost converters the output transistor is shown as an important source of losses when the difference between the drain and source junctions increases (output voltage and switching node of the boost converter). In order to reduce the reverse losses of the converter, an innovative boost-converter topology is proposed: two TFET devices in series operate as output transistors, with a voltage applied between them when they are reverse biased. The proposed solution shows improved performance at large conversion ratios when compared to the conventional inductor-based boost converter.

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REFERENCES

[1] P.-H. Hsieh, C.-H. Chou, and T. Chiang, "An RF energy harvester with 44.1% PCE at input available power of -12 dBm," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1528–1537, Jun. 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7112586/

[2] G. A. Rincón-Mora and S. Yang, "Tiny piezoelectric harvesters: Principles, constraints, and power conversion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 5, pp. 639–649, May 2016.

[3] G. Bassi, L. Colalongo, A. Richelli, and Z. M. Kovacs-Vajna, "100 mV–1.2 V fully-integrated DC–DC converters for thermal energy harvesting," *IET Power Electron.*, vol. 6, no. 6, pp. 1151–1156, Jul. 2013.

[4] U. Çilingiroğlu, B. Tar, and C. Özmen, "On-chip photovoltaic energy conversion in bulk-CMOS for indoor applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2491–2504, Aug. 2014.

[5] E. J. Carlson, K. Strunz, and B. P. Otis, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.

[6] P.-S. Weng, H.-Y. Tang, P.-C. Ku, and L.-H. Lu, "50 mV-input batteryless boost converter for thermal energy harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1031–1041, Apr. 2013.

[7] D. El-Damak and A. P. Chandrakasan, "A 10 nW–1 μW power management IC with integrated battery management and self-startup for energy harvesting applications," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 943–954, Apr. 2016.

[8] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanocurrent power management IC for low-voltage energy harvesting sources," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4292–4304, Jun. 2016.

[9] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[10] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014.

[11] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88–95, May 2015.

[12] Y.-N. Chen, M.-L. Fan, V. P.-H. Hu, P. Su, and C.-T. Chuang, "Evaluation of sub-0.2 V high-speed low-power circuits using heterochannel MOSFET and tunneling FET devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 12, pp. 3339–3347, Dec. 2014.

[13] D. Cavalheiro, F. Moll, and S. Valtchev, "Pespectives of TFET devices in ultra-low power charge pumps for thermo-electric energy sources," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Lisbon, Portugal, May 2015, pp. 1082–1085. [Online]. Available: http://ieeexplore.ieee.org/articleDetails.jsp?arnumber=7168825

[14] H. Liu *et al.*, "Tunnel FET RF rectifier design for energy harvesting applications," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 4, pp. 400–411, Dec. 2014.

[15] D. Cavalheiro, F. Moll, and S. Valtchev, "TFET-based power management circuit for RF energy harvesting," *IEEE J. Electron Devices Soc.*, vol. 5, no. 1, pp. 7–17, Jan. 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7742921/

[16] H. Liu, V. Saripalli, V. Narayanan, and S. Datta. (Apr. 2015). *III-V Tunnel FET Model*. [Online]. Available: https://nanohub.org/publications/12/2

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